Title: GENERATING ADJUSTABLE-DELAY CLOCK SIGNAL FOR PROCESSING COLOR SIGNALS
Inventor: Ha Chu Vu
Docket No.: 08211/0200375-US0

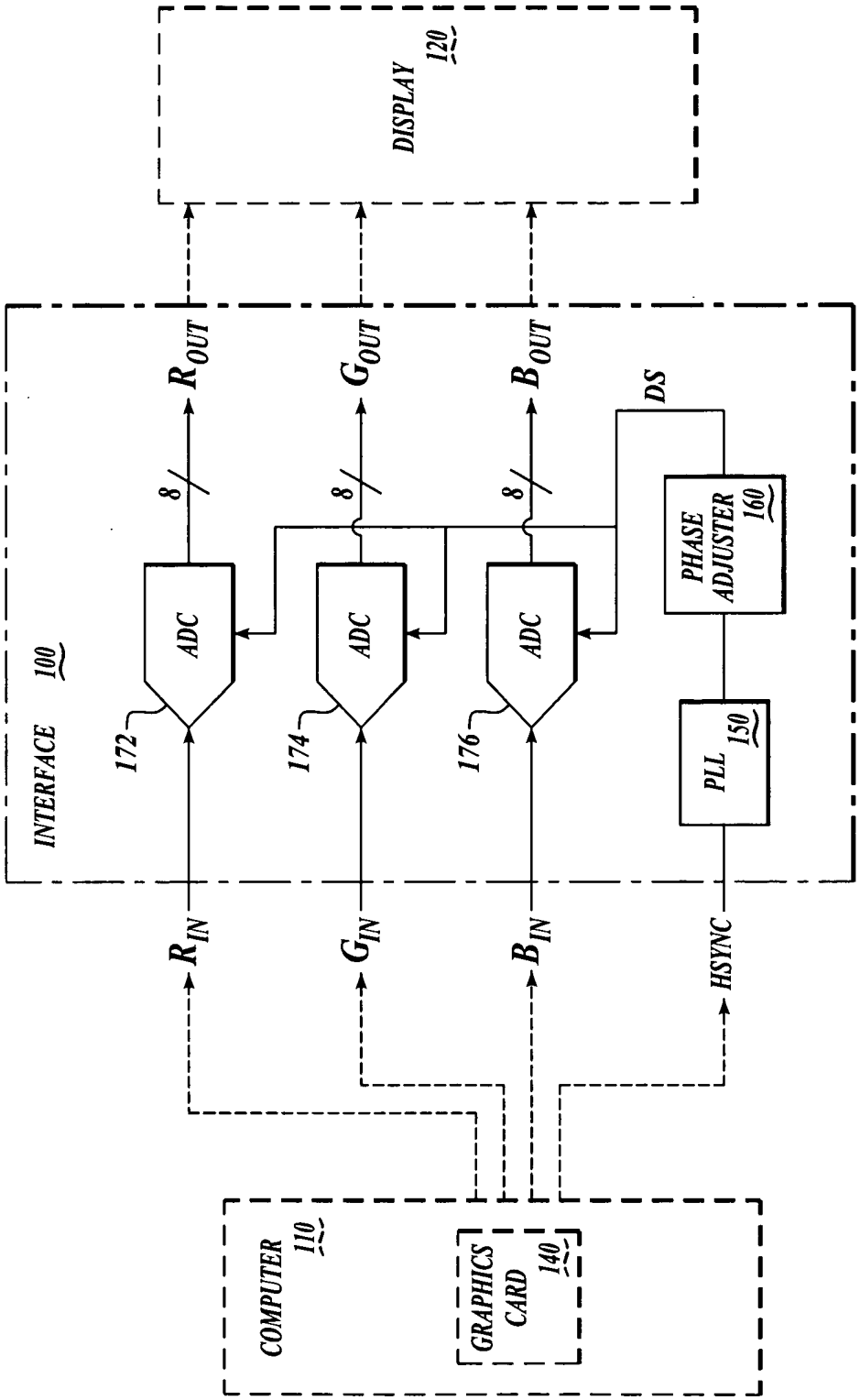


Fig.1

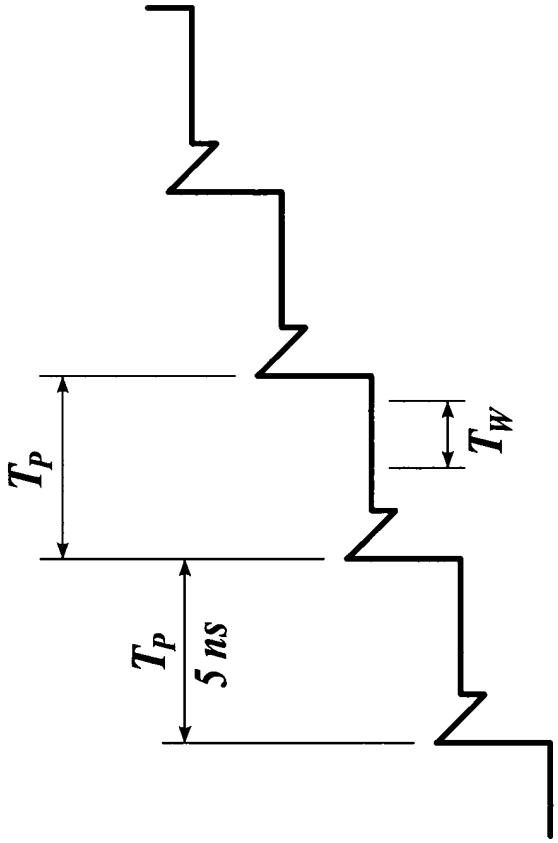


Fig.2

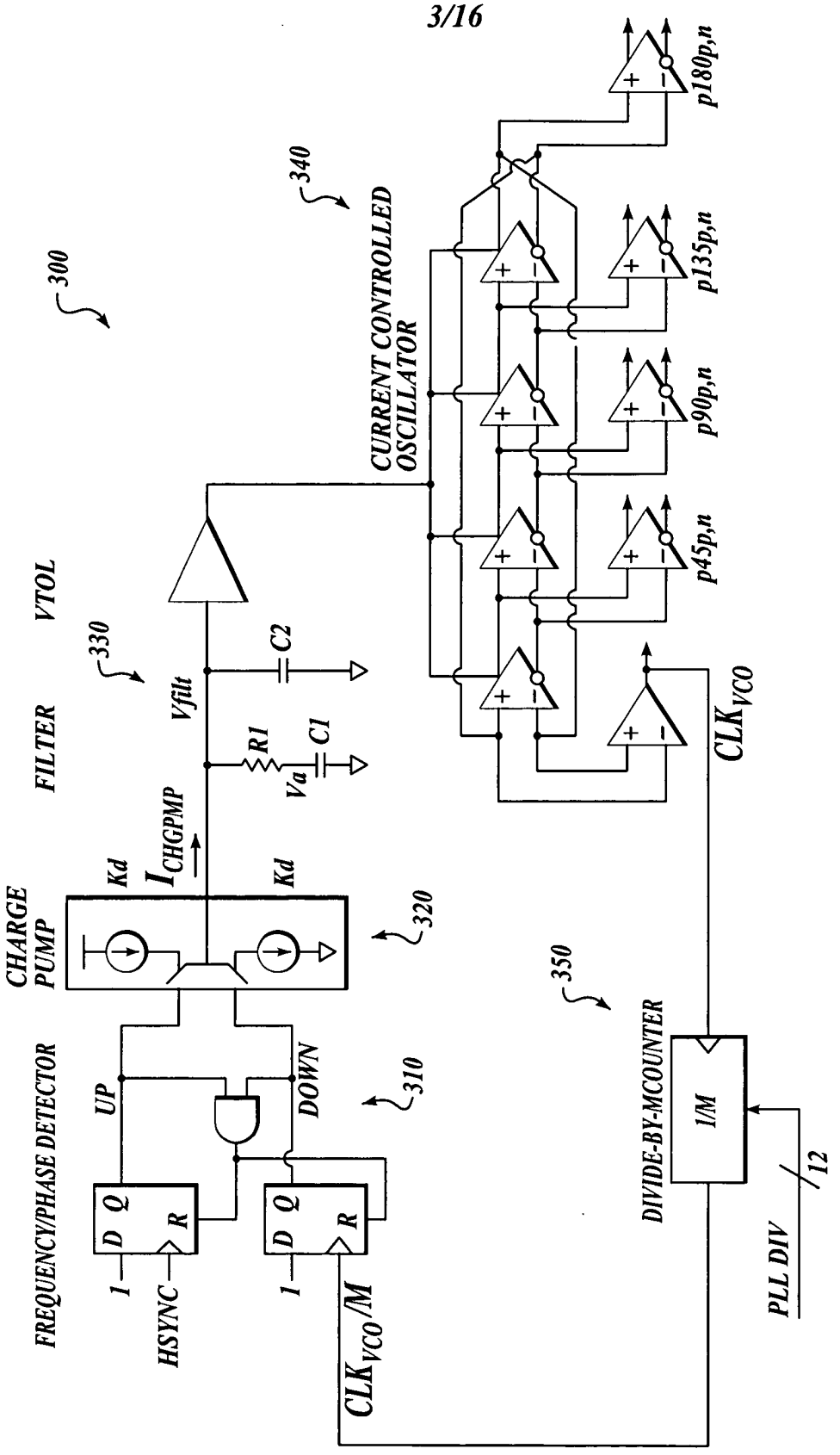

300
340
CURRENT CONTROLLED OSCILLATOR
p180p,n
p135p,n
p90p,n
p45p,n
CLK_{VCO}
330
FILTER
VTOL
Vfilt
C2
R1
C1
Va
I_{CHGPMP}
Kd
Kd
CHARGE PUMP
320
350
DIVIDE-BY-MCOUNTER
1/M
PLL DIV
/12
FREQUENCY/PHASE DETECTOR
UP
DOWN
310
D Q
R
1
HSYNC
CLK_{VCO}/M

Fig.3

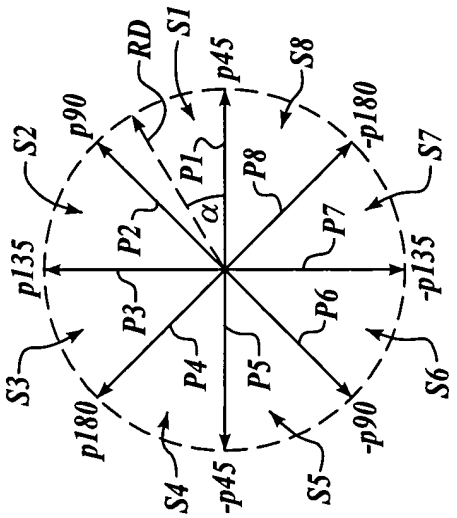

RD
S1
p45
S8
p90
S2
-p180
S7
P1
P8
α
P2
P7
p135
-p135
P3
P6
S3
P4
P5
S6
p180
-p90
S4
-p45
S5

Fig. 4

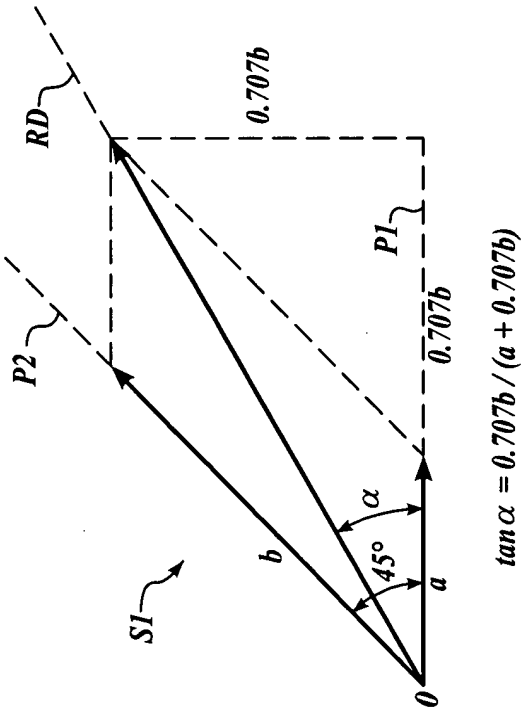


Fig. 5

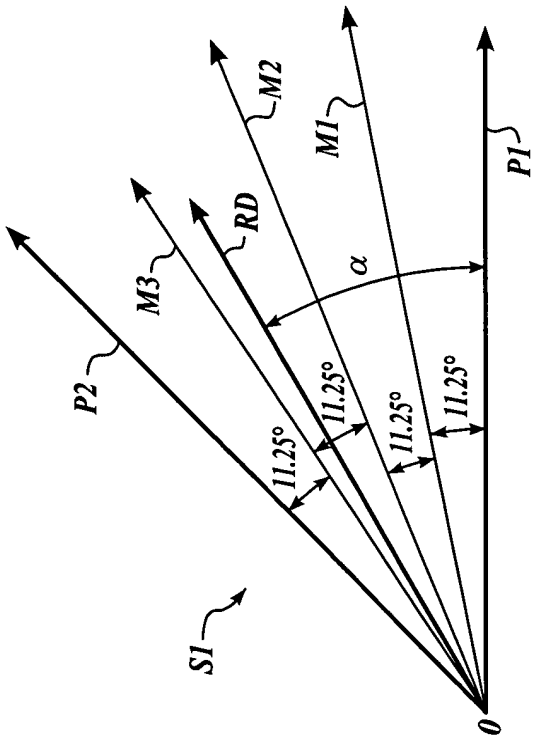
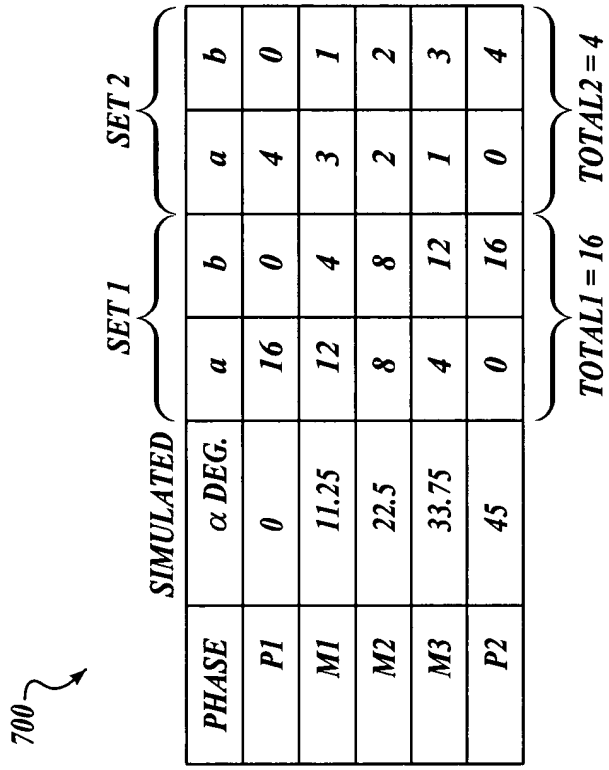
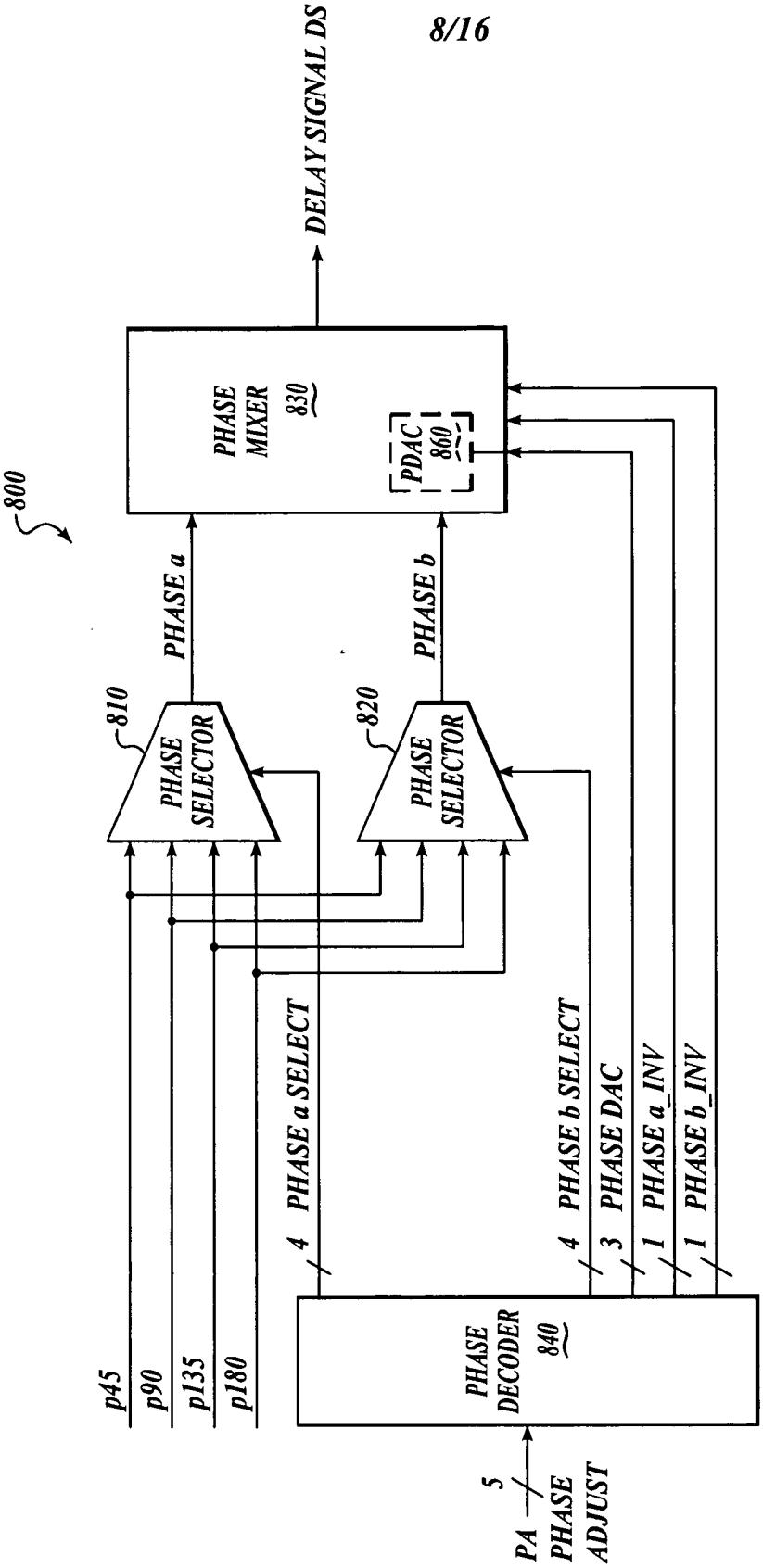


Fig. 6



WEIGHT VALUES FOR SIMULATED PHASES

Fig. 7



PHASE ADJUSTER

Fig. 8

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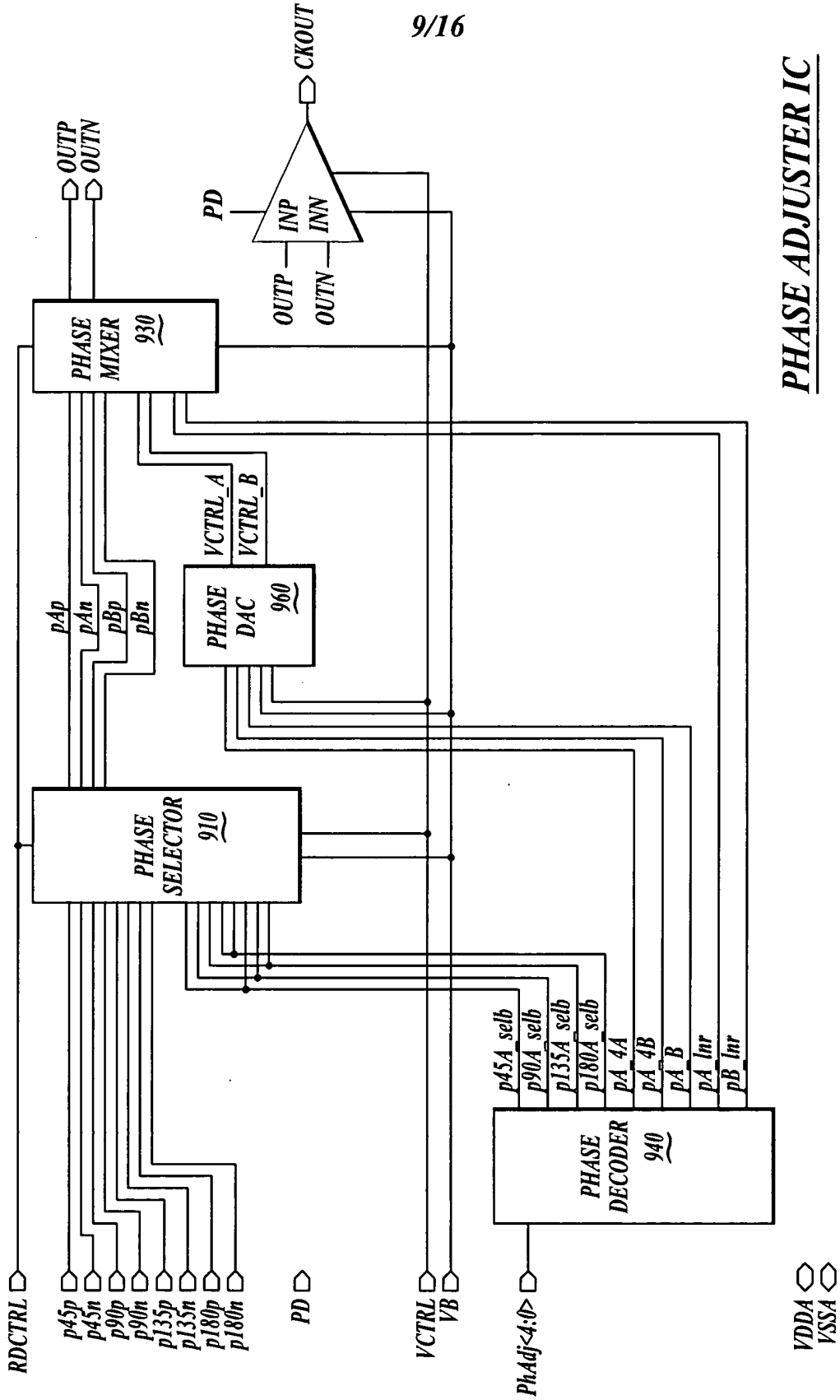


Fig. 9

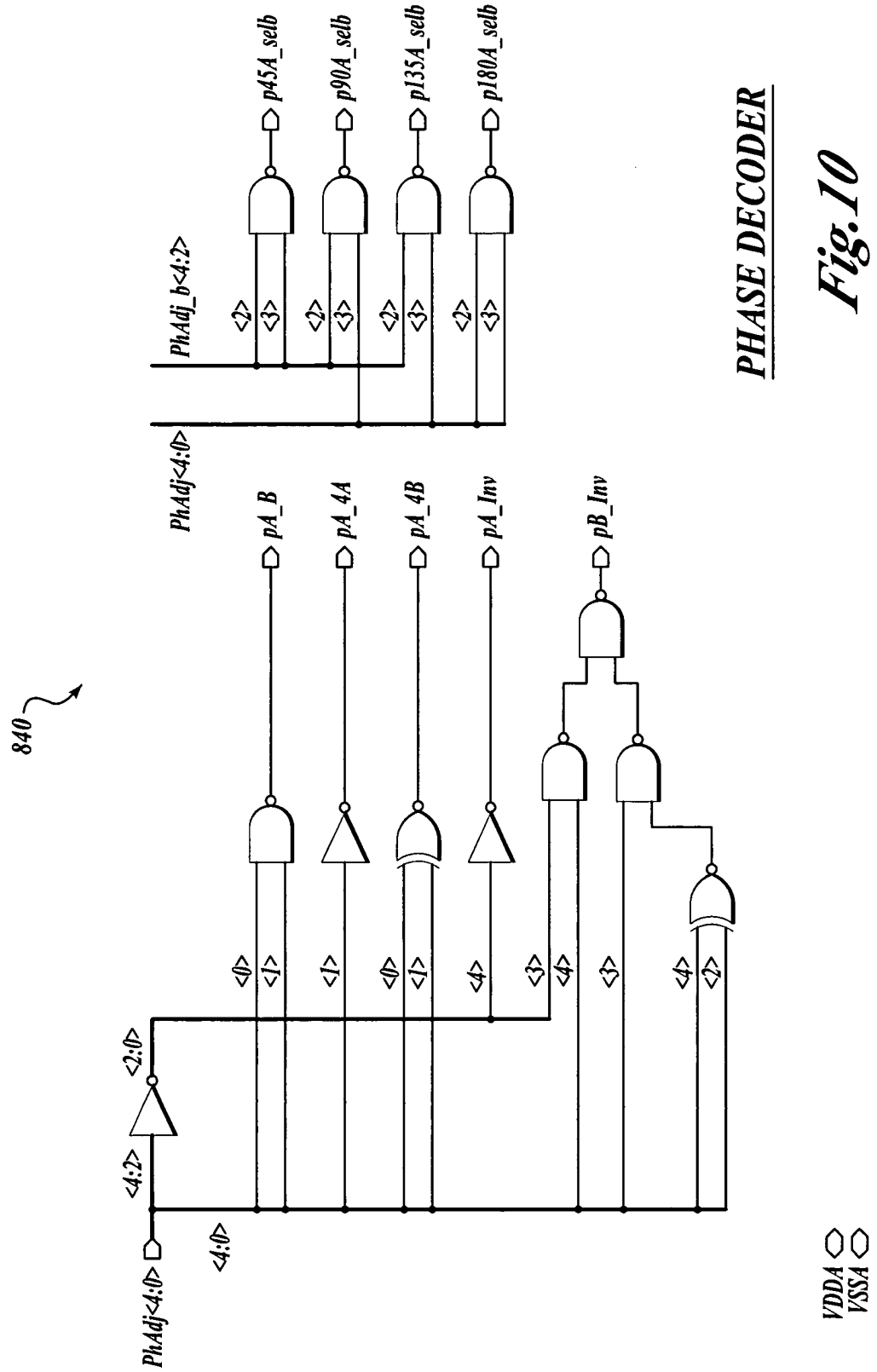

840
PHASE DECODER
PhAdj<4:0>
PhAdj_b<4:2>
p45A_selb
p90A_selb
p135A_selb
p180A_selb
pA_B
pA_4A
pA_4B
pA_Inv
pB_Inv
<2:0>
<4:2>
<4:0>
VDDA
VSSA

Fig. 10

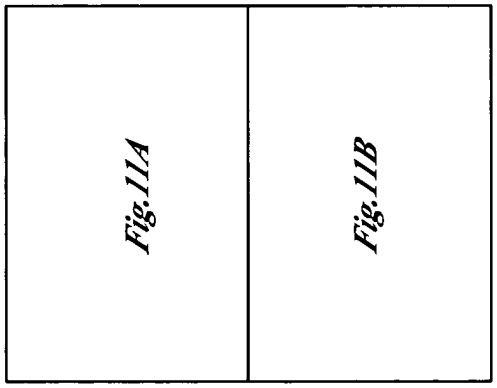
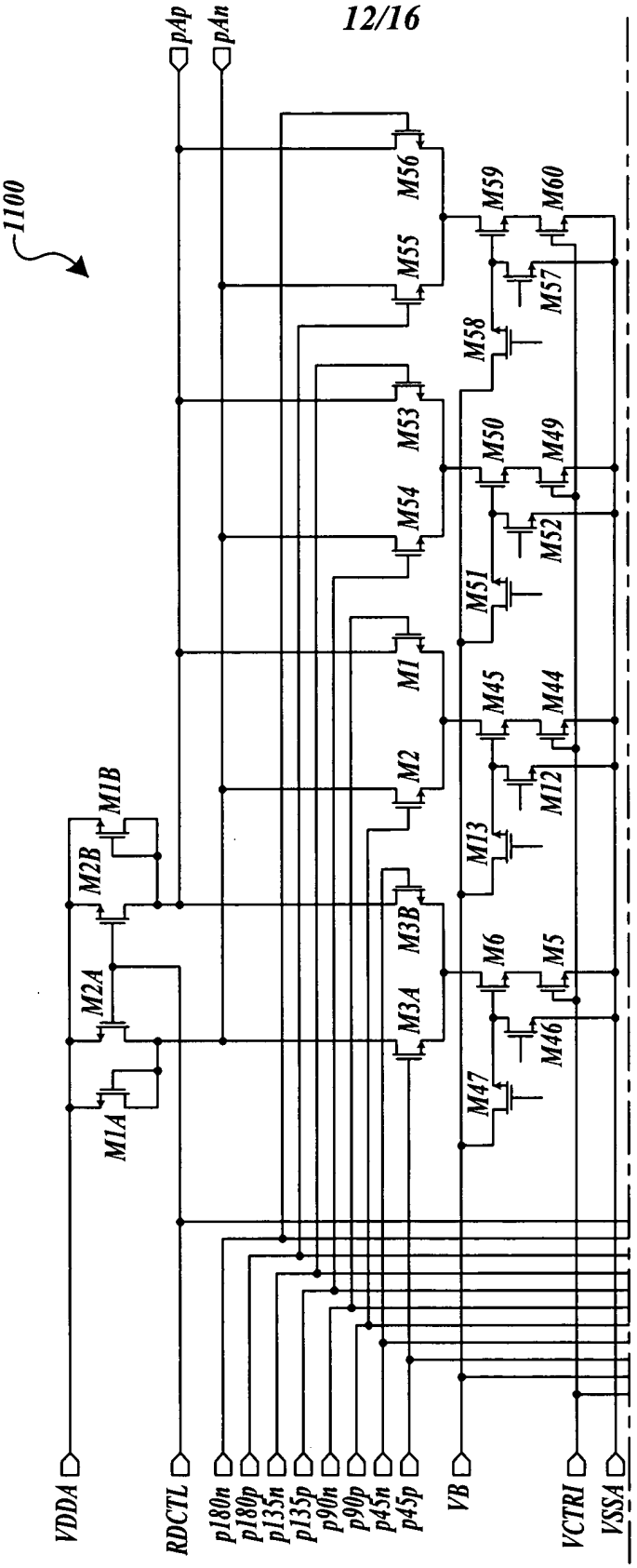


Fig.11



PHASE SELECTOR CHIP

Fig. 11A

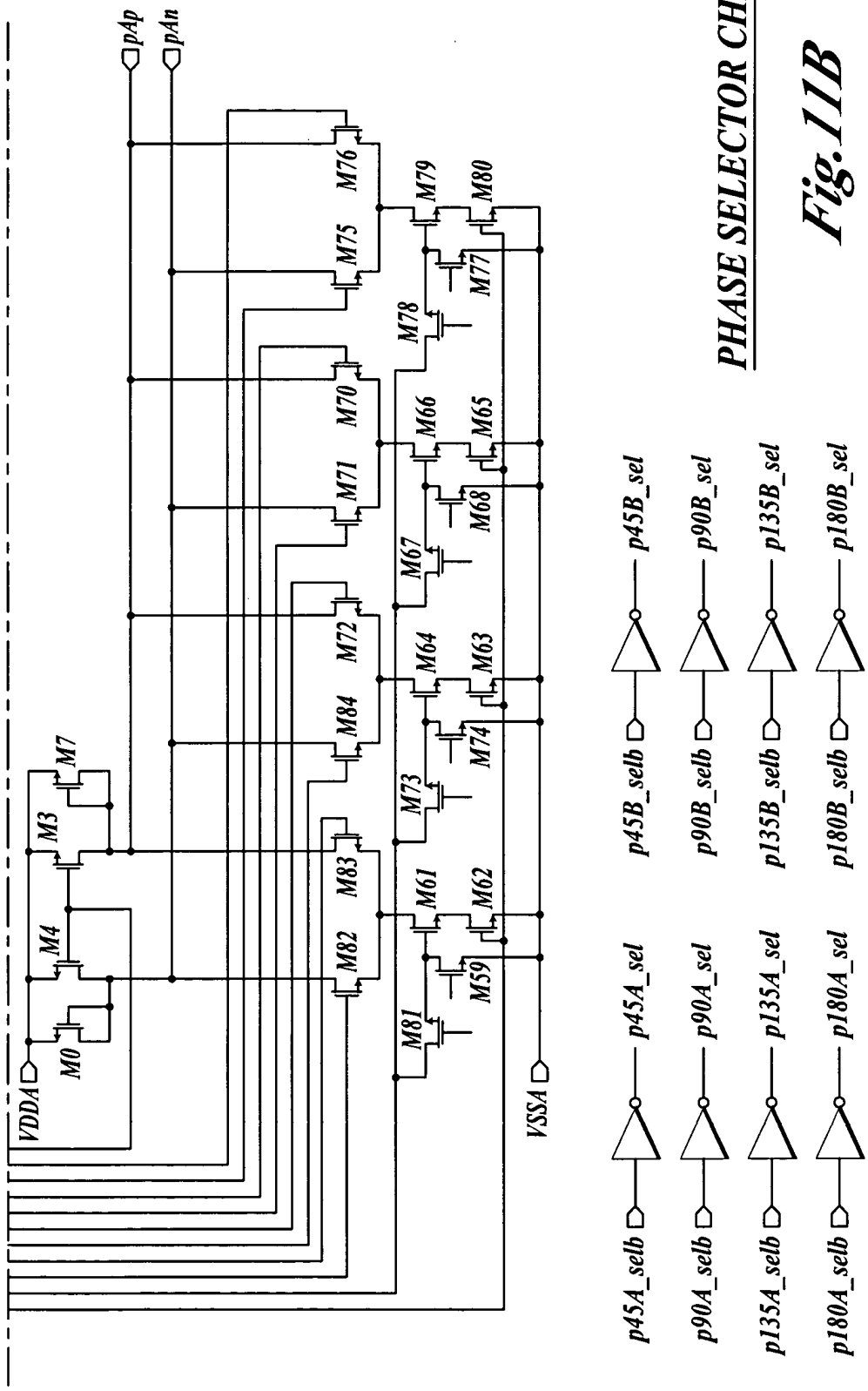
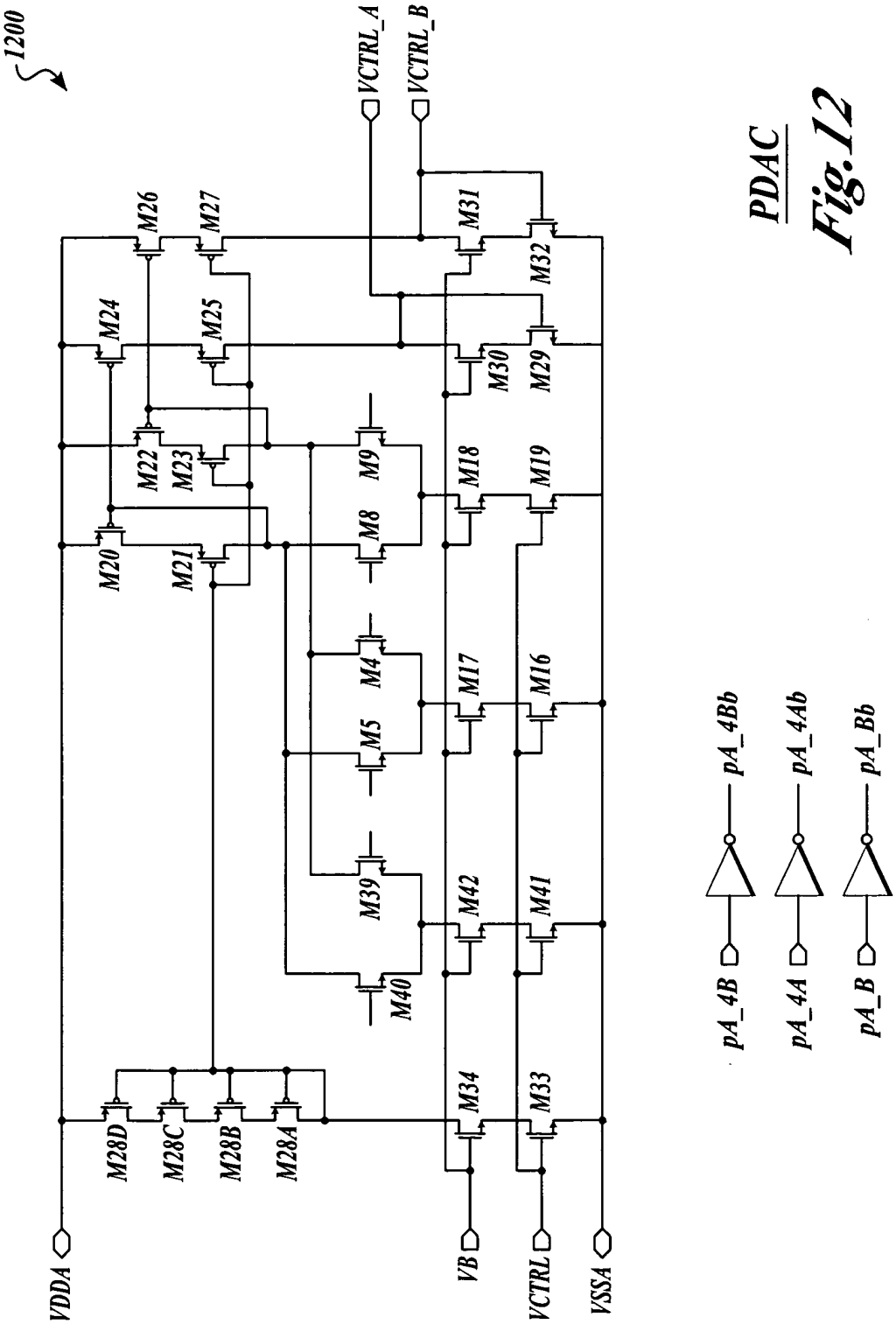

PHASE SELECTOR CHIP
pAp
pAn
VDDA
VSSA
M0
M3
M4
M7
M59
M61
M62
M63
M64
M65
M66
M67
M68
M70
M71
M72
M73
M74
M75
M76
M77
M78
M79
M80
M81
M82
M83
M84
p45A_sel
p45A_selb
p90A_sel
p90A_selb
p135A_sel
p135A_selb
p180A_sel
p180A_selb
p45B_sel
p45B_selb
p90B_sel
p90B_selb
p135B_sel
p135B_selb
p180B_sel
p180B_selb

Fig. 11B


1200
VCTRL_A
VCTRL_B
M26
M27
M31
M32
M24
M25
M30
M29
M22
M23
M9
M18
M19
M20
M21
M8
M4
M17
M16
M5
M39
M42
M41
M40
M34
M33
M28D
M28C
M28B
M28A
VDDA
VB
VCTRL
VSSA
pA_4Bb
pA_4Ab
pA_Bb
pA_4B
pA_4A
pA_B

PDAC

Fig. 12

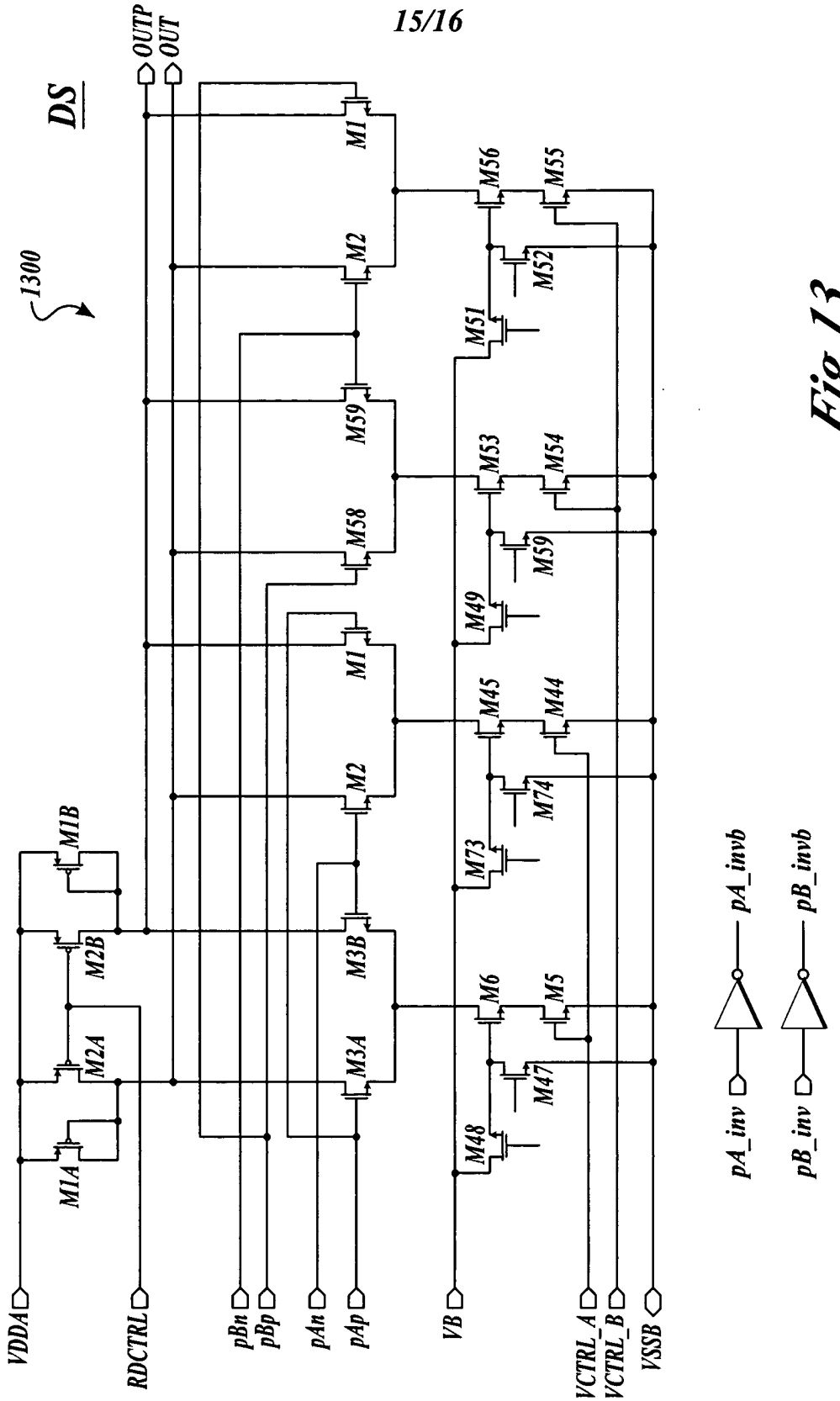

DS
1300
OUTP
OUT
M1
M2
M59
M58
M1
M2
M3B
M3A
M1B
M2B
M2A
M1A
M56
M55
M52
M51
M53
M54
M59
M49
M45
M44
M74
M73
M6
M5
M47
M48
VDDA
RDCTRL
pBn
pBp
pAn
pAp
VB
VCTRL_A
VCTRL_B
VSSB
pA_invb
pB_invb
pA_inv
pB_inv

Fig.13

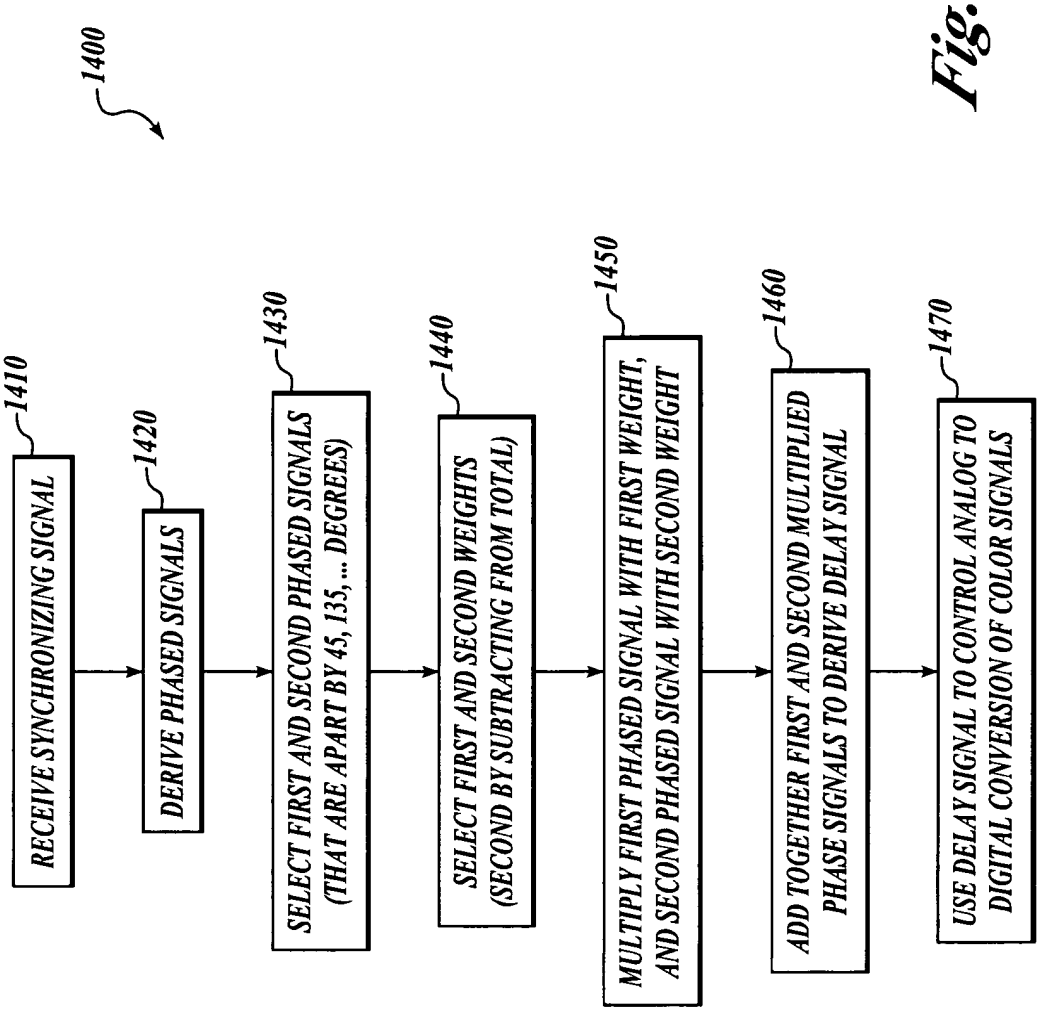

1400
1410
RECEIVE SYNCHRONIZING SIGNAL
1420
DERIVE PHASED SIGNALS
1430
SELECT FIRST AND SECOND PHASED SIGNALS (THAT ARE APART BY 45, 135, ... DEGREES)
1440
SELECT FIRST AND SECOND WEIGHTS (SECOND BY SUBTRACTING FROM TOTAL)
1450
MULTIPLY FIRST PHASED SIGNAL WITH FIRST WEIGHT, AND SECOND PHASED SIGNAL WITH SECOND WEIGHT
1460
ADD TOGETHER FIRST AND SECOND MULTIPLIED PHASE SIGNALS TO DERIVE DELAY SIGNAL
1470
USE DELAY SIGNAL TO CONTROL ANALOG TO DIGITAL CONVERSION OF COLOR SIGNALS

Fig. 14